JMicron Technology Corporation

JMF608
SATA III NAND Flash Controller

Overviews

JMF608 is a single chip SATA III NAND flash controller. It supports up to 4 channels with 4 CE/channel NAND flash memory. JMF608 provides on-chip RAM buffer, optimized for capacity below 128GB, and is suitable to cost effective, small capacity SSD or hard drive cache application. The embedded hardwired logic provides the maximum 300Mbps data read and 200Mbps data write speed to NAND flash memory.

JMF608 has the best supporting to the latest NAND flash memory, including Toshiba 19nm and Micron 20nm Flash. It also provides the hardwired Error Correction Code (ECC) engine (up to 40b/1KB), wear leveling, and bad block management technology in this chip.

JMF608 provides embedded processor, internal masked ROM, data SRAM, SATA link/transport layer, SATA PHY. It supports online firmware upgrade through SATA port. Data swap between different interfaces can be done very efficiency by DMA without CPU intervention.

Features

Whole Chip

- Integrated SATA III port and 4-channel NAND flash memory controller.
- Provides 17 pins GPIO shared by below.
  - SATA access LED indicator.
  - UART
  - 4-wire SPI flash
  - I2C peripheral, such as thermal sensor
  - JTAG port
  - Chip configuration
  - Firmware configurable GPIO
- Built-in power-up self-test (BIST).
- Manual and automatic self-diagnostics.
- External 25MHz crystal oscillator.
- 3.3V/1.8V/1.2V power supply
- 9x9mm^2 143-ball TFBGA package

CPU System

- On-chip 32-bit microprocessor with ARM9 base instruction set.
- On-chip 32KB masked program ROM.
- On-chip 384KB program SRAM.

SATA Controller

- Compliant with Serial ATA International Organization: Serial ATA Revision 3.1.

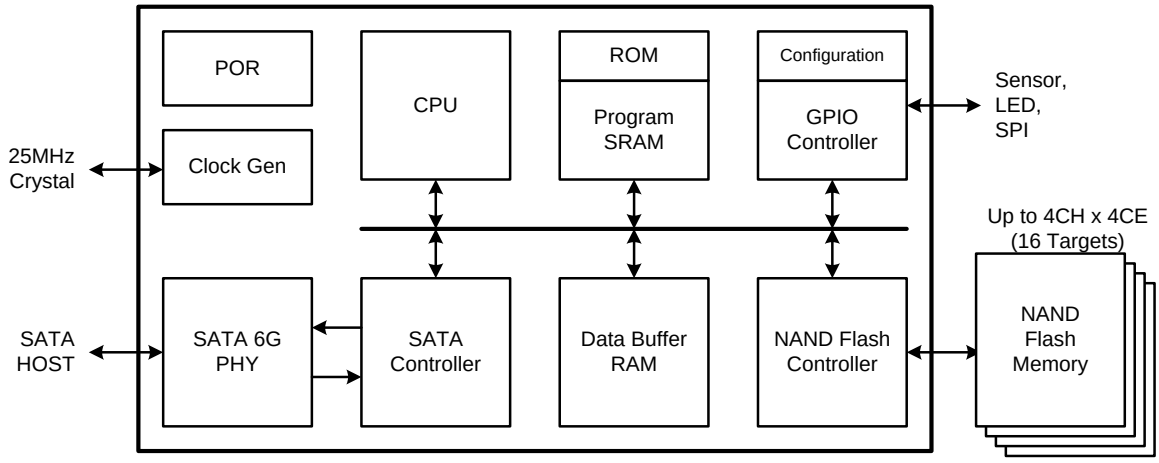
- Supports 1-port 1.5/3.0/6.0Gbps SATA I/II/III interface.
- Support ATA-8 command set
- Supports Partial/Slumber/Device Sleep and dynamic power management.
- Support S.M.A.R.T (Self-Monitoring, Analysis and Reporting Technology).

NAND Flash Controller

- Support 4 hardware channels with 4 CE pins per channel to NAND flash memory.
- On-chip data buffer RAM.
- Support Toshiba 24nm/19nm MLC and Micron 25nm/20nm MLC NAND flash memory.
- Support Legacy/Toggle 1.0/2.0/ONFI 2.3/3.0 NAND flash memory.
- Support up to 300Mbps burst read and 200Mbps burst write to NAND flash memory.
- Enhanced endurance by dynamic/static wear-leveling.
- Supports 8K/16K bytes page size.
- Supports 8/16/24/40-bit per 1KB BCH ECC.
- Support Shift-Read Feature of NAND flash memory

Block Diagram

Figure 1 Block Diagram



Applications

Table 1 Supporting Flash Capacity List

Density Per Flash	NAND Flash CE	Controller Channel	Total Capacity
8G x 8 bits (64Gb)	1	1/2/3/4	8G/16G/24G/32G Bytes
8G x 8 bits (64Gb)	2	4	64G Bytes
8G x 8 bits (64Gb)	4	4	128G Bytes
16G x 8 bits (128Gb)	1	1/2/4	16G/32G/64G Bytes
16G x 8 bits (128Gb)	2	4	128G Bytes